Amendments to the Claims

The current listing of the claims replaces all previous amendments and listings of the claims.

1. (Currently Amended) ~~A grid array~~ An electronic component ~~in which~~ comprising:

~~a grid array LSI chip having a large number of~~ a semiconductor comprising first lands electrically connected to ~~a large number of~~ second lands ~~through connecting means~~, said ~~latter~~ second lands ~~are~~ connected to ~~a wire~~ wires of a ~~printed wiring~~ board,

wherein at least one of the second lands comprises a primary land and an auxiliary land ~~is formed at a connection portion of said land connecting a wiring pattern at a portion,~~ the at least one second land connecting to at least one of the wires where ~~an excessive~~ a predetermined tensile stress is configured to be applied between said ~~lands on the printed wiring board corresponding to said grid array LSI chip~~ at least one second land and ~~said wiring pattern as~~ said at least one wire,

the primary land comprises an arcuate shape, and

the auxiliary land comprises a first portion disposed adjacent the primary land and a second portion connecting to the at least one wire, the first portion having a greater cross sectional area than the second portion.

2. (Currently Amended) The ~~grid array~~ electronic component according to claim 1, wherein said auxiliary land is ~~formed at said land located on at least a portion~~ configured to be disposed where ~~an excessive~~ the predetermined tensile stress ~~as compared with another portion of the printed wiring board~~ is applied when a load is applied to said ~~printed wiring~~ board.

3. (Currently Amended) The ~~grid array~~ electronic component according to claim 2, wherein said auxiliary land ~~is formed at said land located on a portion corresponding to~~

electrically connects with at least one of the first lands at a corner ~~portion of said grid array LSI chip in said printed wiring board~~ of the semiconductor.

4. (Currently Amended) The ~~grid array~~ electronic component according to claim 2, wherein said auxiliary land ~~is formed at the land located on a portion corresponding to~~ electrically connects with at least one of the first lands at an end ~~of an IC chip disposed in said grid array LSI chip in said printed wiring board~~ of an integrated circuit of the semiconductor.

5. (Currently Amended) The ~~grid array~~ electronic component according to claim 2, wherein said auxiliary land is ~~formed at said land connected to said wiring pattern which is formed~~ configured to be disposed so as to extend in a direction in which a warpage of said ~~printed wiring~~ board is generated ~~and in a direction closer to the former direction in a ref low soldering step of said grid array electronic component~~.

6. (Currently Amended) The ~~grid array~~ electronic component according to claim 2, wherein said auxiliary land is ~~formed at the land in which an excessive~~ configured to be disposed where the predetermined tensile stress is applied ~~to said wiring pattern in a correcting step which corrects warpage and~~ during correction of a distortion of said ~~printed wiring~~ board ~~or an assembly step~~ during an assembly of the semiconductor to the board.

7. (Currently Amended) The ~~grid array~~ electronic component according to claim 2, wherein said auxiliary land ~~is formed so that a connection cross section area from said land of said printed wiring board corresponding to said portion of said land of said grid array LSI chip to said wiring pattern is gradually varied~~ comprises a third portion disposed between the first and second portions, the third portion having a cross sectional area less than the first portion and greater than the second portion.

8. (Currently Amended) The ~~grid array~~ electronic component according to claim 3, wherein said auxiliary land ~~is constituted by an auxiliary land having a different shape in~~

~~accordance with a position of said land of said printed wiring board corresponding to said land of said corner portion of said grid array LSI chip~~ has a shape determined based on a position of the auxiliary land in relation to a corner of the semiconductor.

9. (Currently Amended) The ~~grid array~~ electronic component according to claim 3, wherein said auxiliary land ~~is constituted so that an average value of a connection cross section area of a land closer to the printed wiring board corresponding to the land closer to an end of the corner portion of said grid array LSI chip becomes larger~~ comprises an arcuate shape.

10. (Currently Amended) The ~~grid array~~ electronic component according to claim 2, wherein ~~said~~ the at least one second land comprises a second auxiliary land ~~is formed at a connection portion around a~~ disposed adjacent a through hole ~~connected to the wiring pattern on an inner layer printed wiring board of a multilayer printed wiring board constituting said printed wiring board~~.

11. (Currently Amended) The ~~grid array~~ electronic component according to claim 3, wherein ~~said wiring pattern connected to said land formed with said auxiliary land of said printed wiring board corresponding to a corner portion of said grid array LSI chip is connected to a connection portion formed with an auxiliary land of~~ the at least one second land comprises a second auxiliary land disposed adjacent a via hole on said ~~printed wiring~~ board.

12.-15. (Canceled)

16. (Currently Amended) ~~A grid array~~ An electronic component ~~in which~~ comprising:

~~a grid array LSI chip having a large number of~~ a semiconductor comprising first lands electrically connected to ~~a large number of lands through connecting means~~ second lands, said ~~latter~~ second lands ~~are~~ connected to ~~a wire~~ wires of a ~~printed wiring~~ board,

wherein at least one of the second lands comprises a primary land and an auxiliary land ~~whose connection cross sectional area is increased is formed on a connection portion of said land connecting a wiring pattern at a portion~~, the at least one second land connecting to at least one of the wires where ~~an excessive~~ a predetermined tensile stress is configured to be applied between ~~a land in a printed wiring board corresponding to said grid array LSI chip and said wiring pattern which is taken outward to be connected to a via hole as said wire~~ the at least one second land and the at least one wire,

the primary land comprises an arcuate shape, and

the auxiliary land comprises a first portion disposed adjacent the primary land and a second portion connecting to the at least one wire, the first portion having a greater cross sectional area than the second portion.

17. (New) An electronic component, comprising:

a semiconductor comprising first and second semiconductor lands;

a board comprising first and second board lands electrically connected to the first and second semiconductor lands, the first board land including a primary portion contacting the first semiconductor land and an auxiliary portion configured to electrically connect to a wire,

wherein the primary portion comprises an arcuate shape, and

the auxiliary portion comprises a first portion electrically connected to the primary portion and a second portion configured to contact the wire, the first portion having a greater cross sectional area than the second portion.

18. (New) The electronic component according to claim 17, wherein the primary portion comprises a circular shape.

19. (New) The electronic component according to claim 17, wherein the auxiliary portion has an about triangular shape.

20. (New) The electronic component according to claim 17, wherein the auxiliary portion has a tapered shape.

21. (New) The electronic component according to claim 17, wherein the auxiliary portion has a tear drop shape.

22. (New) The electronic component according to claim 17, wherein the auxiliary portion has a third portion between the first and second portions, the third portion having a cross sectional area between values of the cross sectional areas of the first and second portions.

Amendments to the Drawings

The attached sheets of drawings include replacement Figs. 18a, 18b, and 19-21 labeled as Prior Art.

Attachment: Replacement Sheets (2)